Amendments

1. (Cancelled).

2. (Currently Amended) ~~The device~~ A device for controlling a setup/hold time of an input signal ~~according to claim 1, further comprising~~ comprising:

a driver for outputting a global bus line control signal by amplifying an output signal from an input buffer;

a signal delay unit for delaying the global bus line control signal selectively connected to the driver;

a decoding unit for outputting a test mode delay signal by decoding a test control signal for determining to control setup/hold time corresponding to the global bus line control signal, a test mode entry signal, and a test mode exit signal;

a delay control unit for controlling the setup/hold time of the global bus line control signal by selectively connecting the signal delay unit to the driver according to a state of the test mode delay signal; and

a first latch for latching the global bus line control signal in synchronous to a clock signal.

3. (Currently Amended) The device for controlling a setup/hold time of an input signal according to claim 2 ~~claim 1~~, wherein the driver comprises an inverter chain including an even number of inverters connected in series for delaying and logically non-reversing the output signal from the input buffer.

4. (Currently Amended) The device for controlling a setup/hold time of an input signal according to claim 2 ~~claim 1~~, wherein the signal delay unit comprises:

a first capacitor unit connected selectively to a first node of the driver controlled by the delay control unit; and

a second capacitor unit connected selectively to a second node of the driver controlled by the delay control unit.

5. (Previously Presented) The device for controlling a setup/hold time of an input signal according to claim 4, wherein the first capacitor unit and the second capacitor unit are MOS capacitors.

6. (Previously Presented) The device for controlling a setup/hold time of an input signal according to claim 4, wherein the delay control unit comprises:

a first delay control unit for delaying the setup/hold time of the global bus line control signal by selectively connecting the first capacitor unit to the first node according to a first state of the test mode delay signal; and

a second delay control unit for advancing the setup/hold time of the global bus line control signal by selectively connecting the second capacitor unit to the second node according to a second state of the test mode delay signal.

7. (Previously Presented) The device for controlling a setup/hold time of an input signal according to claim 6, wherein the first delay control unit comprises a first transmission gate and a second transmission gate for receiving the test mode delay signal through a NMOS gate, and receiving an inversion of the test mode delay signal through a PMOS gate to selectively connect the first MOS capacitor unit to the first node.

8. (Previously Presented) The device for controlling a setup/hold time of an input signal according to claim 6, wherein the second delay control unit comprises a third transmission gate and a fourth transmission gate for receiving the test mode delay signal through a PMOS gate, and receiving an inversion of the test mode delay signal through a NMOS gate to selectively connect the second capacitor unit to the second node.

9. (Previously Presented) The device for controlling a setup/hold time of an input signal according to claim 6, wherein the decoding unit connects the first capacitor unit to the first node by setting the test mode delay signal high when the test control signal is at a high level, and disconnects the second capacitor unit and the second node by setting the test mode delay signal high when the test control signal is at a low level.

10. (Previously Presented) The device for controlling a setup/hold time of an input signal according to claim 9, wherein the decoding unit comprises:

a logic unit for logically operating the test control signal and the test mode entry signal to output a first output signal and a second output signal;

a second latch for latching the test mode delay signal according to the first output signal and the test mode exit signal; and

a third latch for latching the second test mode delay signal according to the second output signal and the test mode exit signal.

11. (Previously Presented) The device for controlling a setup/hold time of an input signal according to claim 10, wherein the logic unit comprises:

a first NAND gate for NANDing the test control signal and the test mode entry signal to output the first output signal; and

a second NAND gate for NANDing the test mode entry signal and inverted of the test control signal to output the second output signal.

12. (Previously Presented) The device for controlling a setup/hold time of an input signal according to claim 10, wherein the second latch comprises a third NAND gate and a fourth NAND gate that are cross-coupled to each other.

13. (Previously Presented) The device for controlling a setup/hold time of an input signal according to claim 10, wherein the third latch comprises a fifth NAND gate and a sixth NAND gate that are cross-coupled to each other.